



Gp 2122
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BT

Docket No. 52478-5617

4-16-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Shuichi Takayama *et al.*

Serial No.: 10/045,802

Filed: October 19, 2001

For: PROCESSOR FOR EXECUTING
INSTRUCTIONS IN UNITS THAT ARE
UNRELATED TO THE UNITS IN WHICH
INSTRUCTIONS ARE READ AND A
COMPILER, AN OPTIMIZATION APPARATUS,
AN ASSEMBLER, A LINKER, A DEBUGGER,
AND A DISASSEMBLER FOR SUCH A
DEBUGGER

Examiner:

Group Art Unit: 2122

April 3, 2003

Irvine, California 92614

RECEIVED

APR 09 2003

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In an attempt to fully comply with the duty of disclosure set forth in 37 C.F.R. § 1.56 and in conformance with 37 C.F.R. §§ 1.97 and 1.98, applicant wishes to bring to the attention of the U.S. Patent Office the following references:

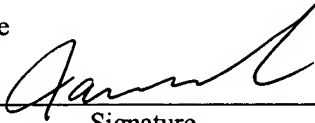
Japanese Laid-open Patent Application No. 4-40525 with English Abstract
Japanese Laid-open Patent Application No. 5-289870 with English Abstract
Japanese Laid-open Patent Application No. 3-48334 with English Abstract
Japanese Laid-open Patent Application No. 3-152624 with English Abstract
Spohrer T., et al.: "Combination PC/Line Prefetch Address Adder," Motorola
Technical Developments, Motorola Inc., vol. 13, 1 July 1991, pages 20-21
U.S. Patent No. 4,040,035
U.S. Patent No. 5,740,447
EP 0 652 510
EP 0 423 726
EP 0 472 025
WO 96 08762

Copies of these references and a form PTO-A820 are attached.

If the Examiner believes that a telephone conference would help further the prosecution of this case, he is respectfully requested to contact the undersigned attorney at the listed telephone number.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on April 3, 2003.

by: James Lee



Signature

Date of Signature: April 3, 2003

Very truly yours,

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